CAN XL physical layer network design

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In automotive and industrial applications, the data communication volume increases and the bit rate in these communication technologies has to be increased too. At the beginning of the CAN story, 1Mbit/s was high a speed bit rate. But now with CAN XL, up to 20Mbit/s in the data phase are possible. Compared with other communication technologies CAN physical layer based on a bus structure and supports collision during communication. The article explains the new CAN SIC XL physical layer concept and the impact on the typical CAN bus topologies.

A very important advantage of CAN is that the CAN physical layer is a physical bus topology and two or more nodes are connected on one physical bus. All nodes on the bus receive the messages at the same time. No switches are needed and there is no propagation delay between the different nodes. To organize such kind of communication, especially at the beginning an arbitration phase is needed. In arbitration phase all nodes transmit a 1 or a 0 on the bus. To make this possible without damaged devices or undefined levels on the bus, only the 0 is actively transmitted on the bus as a dominant signal, while a 1 is passive generated by the termination resistors and is called recessive.

In Figure 1 the Transmitter output behavior is demonstrated and the Transmitter is switching between high impedance to allow recessive level on the bus and dominant to generate a dominant level. The recessive to dominant transition is fully controlled by the transmitter, while during the dominant to recessive transition the maximum possible slew rate is limited only by the Transmitter.

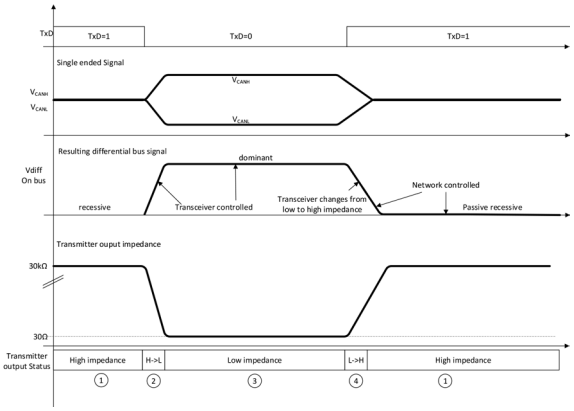


Figure 1: CAN FD Transceiver impedance

The transition is mostly controlled by the wiring harness and the termination resistors. The permanently changing transmitter output impedance during the transmission of dominant and recessive signals the wire doesn't like this and cause a ringing on the network. These ringing limits the maximum possible bit rate in CAN communication. To achieve higher bit rates a modification of the Transmitter concept was needed. With integration of the SIC (Signal improvement capability) Transmitter, a first step was done. In Figure 2 the SIC Transmitter output impedance behavior is shown. The dominant to recessive phase is now controlled by the transmitter too. The output impedance changes now from low impedance in dominant phase to medium impedance of 100 Ohm for max 500ns. This is phase is called active recessive phase. After the active recessive phase, the transmitter output impedance changes from medium to high impedance to allow collision on the bus. This phase is called passive recessive phase. 100 Ohm in the SIC phase was chosen to match the Transmitter impedance with the typical CAN twisted pair wire impedance, which is 100 Ohm.

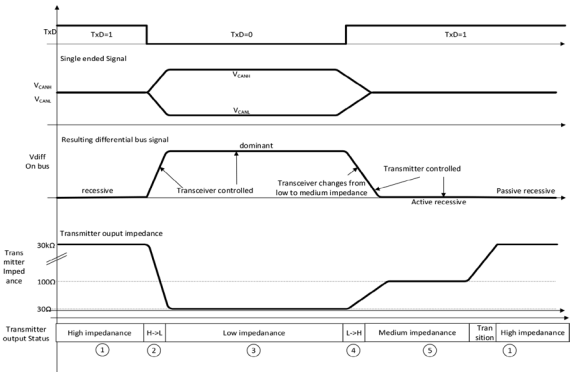


Figure 2: CAN SIC Transceiver Output impedance characteristic

This modification improves the reliability of existing CAN FD networks and allows bit rates up to 8Mbit/s. To achieve bit rates above 8 Mbit/s with CAN XL a new Transmitter concept was needed. In Arbitration phase, the CAN SIC Transmitter concept was chosen and is called SIC Mode and in the data phase the push pull Transmitter concept was chosen to achieve bit rates up to 20 Mbit/s. This mode of the transceiver is called FAST Mode. During ADS Phase of the protocol, the transceiver changes from SIC to FAST mode. The mode change is controlled by the CAN XL controller via TXD pin. The impedance in FAST mode is as well as in active recessive SIC Mode 100Ohm. But due to the alternating waveforms, the symmetry of the transmitted bits is better than in SIC mode and allows bit rates up to 20Mbit/s. In Figure 3 the SIC XL Transmitter impedance characteristic during the SIC to FAST Mode transition and in FAST Mode is shown. The transition starts with a change from

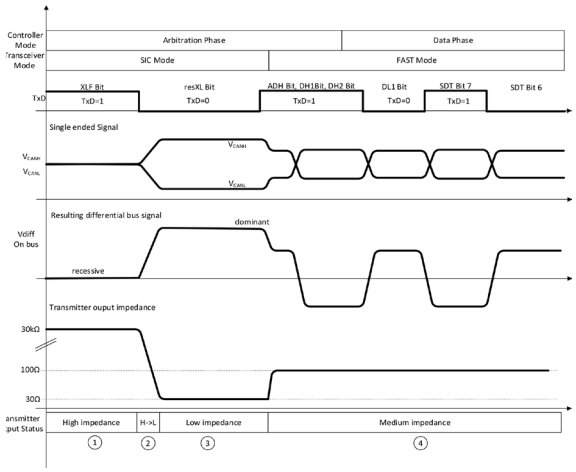


Figure 3: Transmitter impedance characteristic during SIC to FAST mode transition.

dominant level to level 0 and after words to level 1. The change from dominant to level 0 was done to get the same voltage swing like in FAST mode. Otherwise the ringing due to the higher voltage swing must be analyzed in the transition phase separately. In Figure 4 the mode transition from FAST Mode to SIC mode at the end of the data phase is shown. During the complete FAST Mode phase, what is identical with the data phase, the impedance is constant at 100 Ohm and matches with the wire impedance.

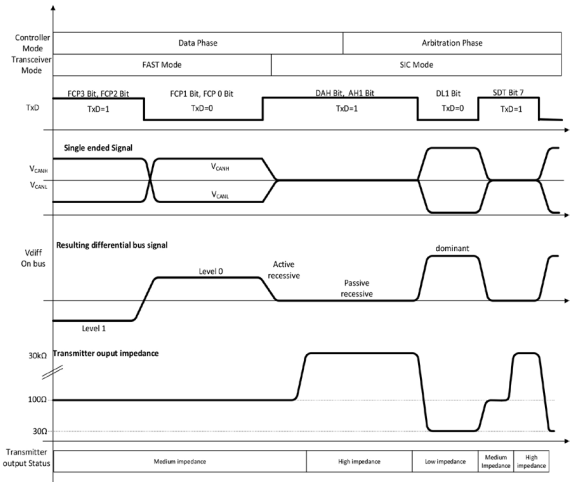


Figure 4: Transmitter impedance characteristic during FAST to SIC mode transition.

Topology investigations

To verify the new physical layer concepts a CAN XL plug fest was done. During the plug fest in January 2023 in Nuremberg, the following topologies were verified.

1.) Point to point network
with different distances between the nodes

Figure 5: Point to Point network

Target:
Verification of the maximum bit rate in a CAN XL Point to Point network

2.) Daisy chain topology like 10BaseT1S
with different distances between the nodes.

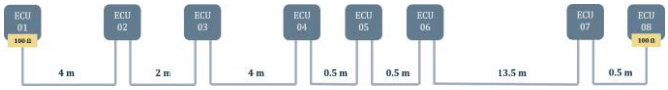


Figure 6: 10BaseT1S like daisy chain topology

Target:
Verification of the maximum bit rate in a daisy chain topology which is similar to 10BaseT1S

3.) CAN like linear topology
with different stub length

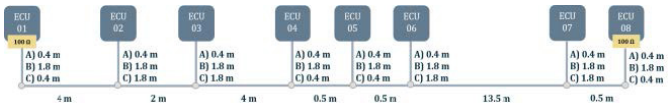


Figure 7: CAN like linear topology

Target:
Verification of the maximum bit rate of a CAN typical linear topology

4.) Single Star Topology

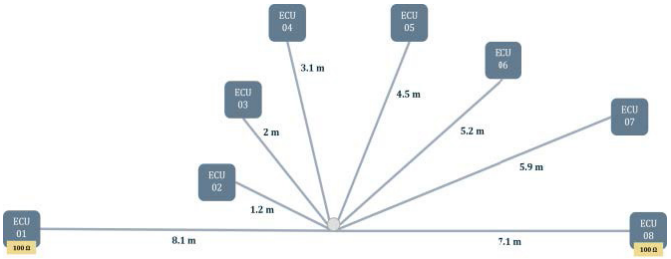


Figure 8: Star Topology

Target:
Verification of the maximum bit rate in a typical CAN star topology with different stub length

5.) Multi Start Topology

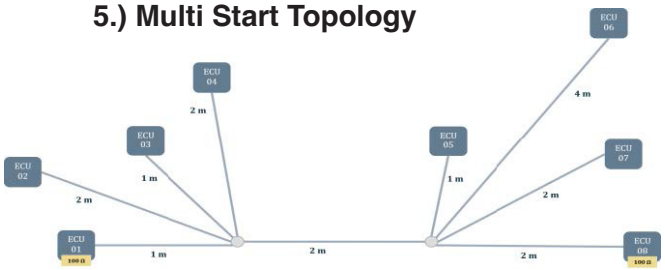


Figure 9 Multi Star Topology

Target:
Verification of the maximum bit rate in a complex CAN star Topology with stub length of 1m, 2m, 4m

The verified pattern

The most critical scenarios in the CAN XL frame are

- The transition SIC to FAST Mode
- A burst of short bits
- A short bit after a long level 0 or level 1 phase (maximum 11 bits acc to the Stuff bit rules) with the opposite level.

1. ADS Transition

During ADH bit, the transmitter switches from dominant to level 0 and afterword's to level 1 and in parallel all receiving nodes change the receiver thresholds. This will be happened by PWM coded symbols send from the CAN XL controller to the TXD Pin of the Transceiver. Before the PWM coded symbol on the TXD pin is detected the receiving nodes transmit a short dominant pulse followed by a shortened SIC phase.

The requirement is, that level 1 is stable before the SDT field starts. Also, the length of the DL1 bit is of interest. The transition DH2 to DL1 is used for resynchronization of the CAN XL controller after the transition into data phase. Also, Level 0 should be achieved. In the SDT field a 0101 pattern was chosen to analyze the impact of short bits in case of high bit rates.

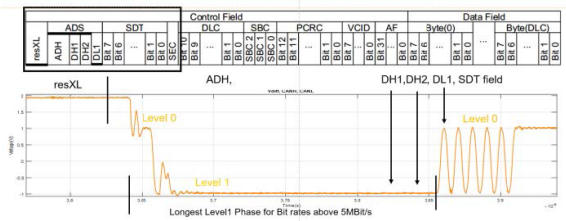


Figure 10 SIC to FAST transition during ADS field

2. Variation of different bit length

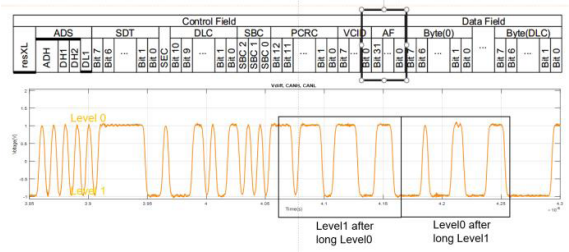


Figure 11: 1,2,3 Bits after long Level 0 or 1

A long phase (4 consecutive bits) followed by short bits (1bit, 2bits or 3bits) with the opposite level. The target was to find out, how long it takes until the bus signals are stable, especially at high bit rates.

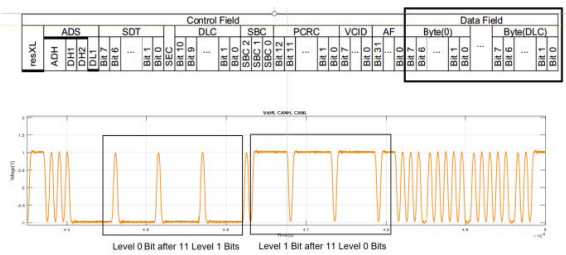


Figure 12: Level 1 or Level 0 Bit after long Phase

The bit lengths are measured after longer level 0 or level 1 phase and the impact of the length of the following bits 1 bit after 11 consecutive Level 1 or Level 0 bits (highest possible number of consecutive bits). The target was to find out, how the bit length and the level behave after the longest possible phase in the frame.

The test criteria

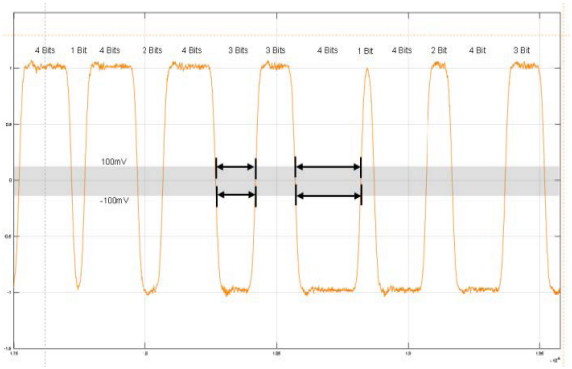


Figure 13: test criteria timing

The bit time lengths were measured at +100mV and -100mV threshold. The bit time should be close to the nominal bit time or multiple of them. For high bit rates the 0V threshold was used. Glitches with a length of 20ns were ignored.

The results

Topology 1:
Point to point network
Topology 1c with 5m distance
Bit rate 20Mbit/s

Figure 14: Test Topology 1c

In Figure 14 the test topology is shown. It was a Point to point topology with 5m wire length between the nodes. In Figure 15 the bus differential signal of the full (and in this test short) FAST phase is shown; no reflection or jitter were observed and the levels of level 0 and level 1 are independent of the bit length.

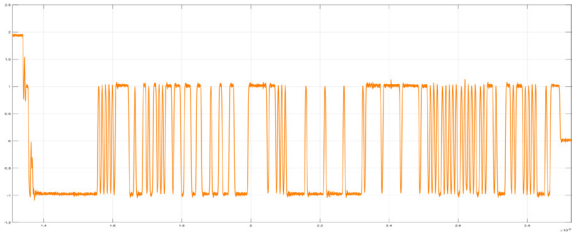


Figure 15: full FAST phase (differential bus signal)

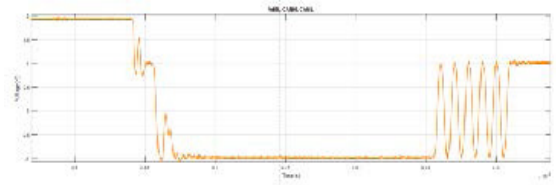


Figure 16: ADS phase and SDT phase

In Figure 16 the critical ADS phase, consisting of ADH bit (2000ns long, DH1 and DH2 bit (each 50ns long), is shown. At the beginning of the transition from dominant to level0 a short SIC phases of the transmitting node can be seen, before the Transceiver has the new PWM coding detected. The length and the voltage swing of these spike depends on the duty cycle ratio of the PWM symbol. After the transition to level 1 the short spike is coming from the receiving node. On the receiving node also PWM coding start to set the Transceiver in FAST mode. Before the Transceiver is able to detect PWM coding on its TXD Pin, a short dominant pulse followed by a shortened SIC phase is transmitted. The spikes during the transition from level 0 to level 1 are very short and also the level 1, level 0 pattern in the SDT field are without any observations.

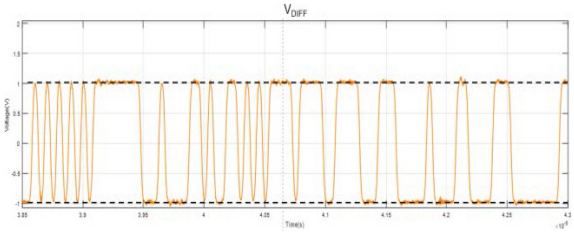


Figure 17: Different pattern in FAST mode

In Figure 17 pattern variations are shown. The max level on single bits of level 0 or level 1 are achieved but short. In the test prototype samples were used. The slew rates of the final Transceiver might be faster and the max level phase during a single bit longer.

Result:
Levels in FAST mode and pulse (bit) lengths are symmetric.
20 Mbit/s pass

Topology 3:
10BaseT1S like linear topology

Scenario 1:
Node 7 transmitting, node 7 observation
Bit rate 20 Mbit/s

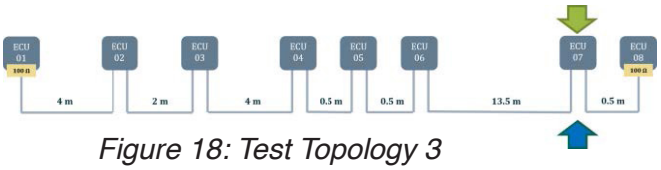


Figure 18: Test Topology 3

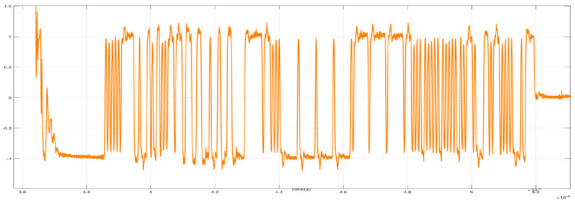


Figure 19: full FAST phase on node 7

Voltage level of short bits doesn't achieve the max levels of Level 0 and Level1.
Small but acceptable bit time degradation observed.

Result:
Pass at 20 Mbit/s
The result based on these results only. Temperature dependencies and Wire Impedance variations are not considered and should be verified separately

Scenario 2:
Bit rate 20Mbit/s
Node 3 transmitting, node 7 observation

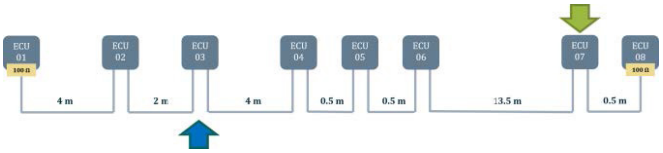


Figure 20: Test Topology 3 transmitting node 3

In this test setup the impact of the distance between Transmitter and Receiver should be analyzed. The parasitic Caps on the ECUs, the number of star points, the high number of untwisted parts and the long distance between the Transmitter and Receiver with 28m was of interest. The transmitter transmits the pulse (bit) at first into the wire impedance of 100Ω, with a delay the impact of the termination on node 1 (delay round about 40ns (7m*5,5ns)) can be observed and with a delay of 120ns (20m*5,5ns) can be seen. The single bit bursts are the most interesting situation during the frame.

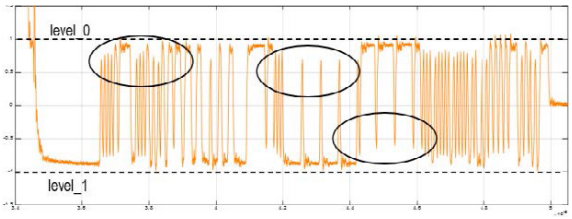


Figure 21: full FAST phase Node 3 transmitting

The longer distance between transmitting and receiving node caused lower Voltage levels of short bits and doesn't achieve the max levels of Level 0 and Level1. The bit length is smaller but close to the minimum bit length. In the single bit burst a king of pumping can be seen. The first bit level is lower than the second and third one, caused by the capacitive load. The capacitance on the ECUs should be as small as possible. The critical situation is the single bit after multiple bits with the same level. The level has an acceptable distance to 100mV, the max level of the Receiver threshold. The impact of temperature dependencies, wire impedance variation due to production and mechanical stress. Also, the overall length of the untwisted part has an impact on the max levels and the bit length symmetry.

Small but acceptable bit time degradation

Results:
Pass at 20Mbit/s

Scenario 3:
Bit rate 20Mbit/s
Node 8 transmitting, node 7 observation

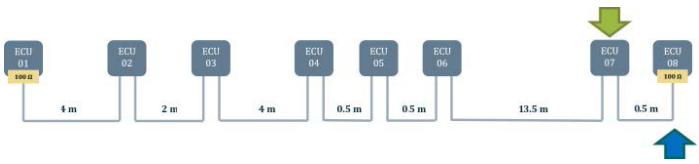


Figure 22: Test Topology transmitting Node 8

In this scenario the impact of a termination node was of interest. The impedance scenario of the transmitting node is different to the unterminated node. The transmitter is directly connected to the 100 Ohm termination resistor and in parallel with the 100 Ohm impedance of the wire. The impact of the second termination located in node 1 can be observed after 150ns during the third bit. The Waveforms on Node 7 are more or less the same as on node 8 due to the short distance between both nodes. Voltage level of short bits doesn't achieve the max levels of Level 0 and Level1

Small but acceptable bit time degradation

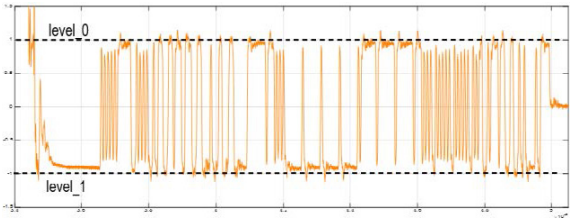


Figure 23: full FAST phase of Node 8 transmitting

The long wire length, the number of nodes, the parasitic capacitances and the untwisted parts caused that the voltage levels of short bits doesn't achieve the max level of Level 0 and Level1. The bit lengths were shortened but close to nominal bit time. In the test the used prototypes don't fulfill all requirements, especially the slew rate condition. With final silicon the results might be better.

Small but acceptable bit time degradation

Result:
Pass at 20Mbit/s

Topology 5a:
CAN like linear topology with 40cm stub length

Scenario 1:
Bit rate 20Mbit/s
Node 1 Transmitting, Node 8 Observation

Figure 24: Test Topology 5a

The difference to the daisy chain network are the 6 stars, which cause reflection due to impedance mismatch and the high number of untwisted parts (in total 26, one per ECU and 3 per start point). The impact of the signal integrity due to the high number of mismatches compared with the daisy chain network with the same cumulated wire length. In scenario the both terminated nodes are analyzed.

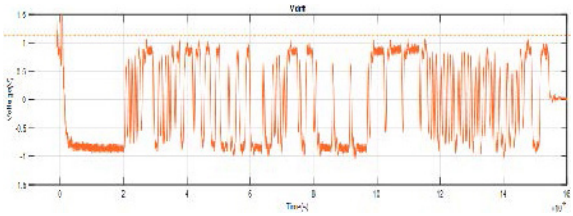


Figure 25: full FAST phase Node 1 transmitting

The Voltage levels of short bits in the SDT field or in after long level 0 of level 1 phased doesn't achieve the max levels of Level 0 and Level1. The levels are lower than in the daisy chain network. The max levels become closer to the Receiver Thresholds. The bit lengths were shortened but close to the nominal bit time. All CAN XL protocol handler were able to detect all frames. In this test the results were acceptable.

Small but acceptable bit time degradation

Result:
Pass at 20Mbit/s

In high volume applications temperature dependencies and wire impedance variation due to fab variation or mechanical stress has to be analyzed.

Scenario 2:
Bit rate 20Mbit/s
Node 3 Transmitting, Node 4 Observation

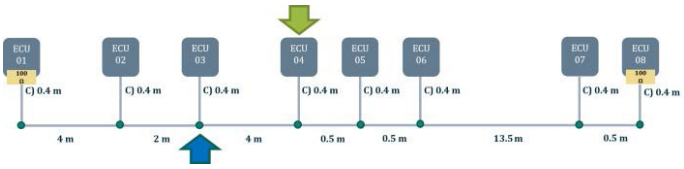


Figure 26: Test Topology 5b

In this scenario two unterminated nodes with 4m difference were analyzed. In Figure 27 the results are shown.

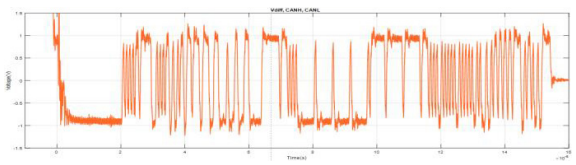


Figure 27: full FAST phase Node 3 transmitting

Compared with the terminated nodes the voltage levels especially in the single bit bursts are higher and the bit timings are closer to the nominal bit time. Pump effects could not be observed. But the voltage levels of short bits don't achieve the max levels of Level 0 and Level1 but the distance to the Receiver thresholds are higher compared with the results on the terminated nodes.

Small but acceptable bit time degradation

Result:
Pass at 20Mbit/s

Scenario 3:
Bit rate 20Mbit/s
Node 6 Transmitting, Node 8 Observation

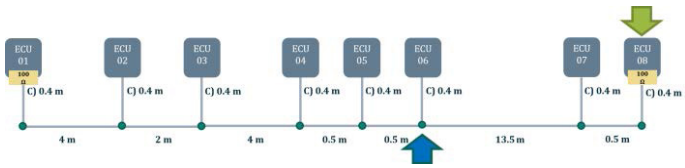


Figure 28: Test Topology 5a, Node 6 transmitting

In scenario 3 the transmitting node is unterminated and the observation node is terminated. The results can be compared with scenario 1 and 2. In Figure 29 the waveforms on node 8 are shown. The voltage levels of short bits don't achieve the max levels of Level 0 and Level1 but are higher than in scenario 1 and lower than in scenario 2.

Small but acceptable bit time degradation

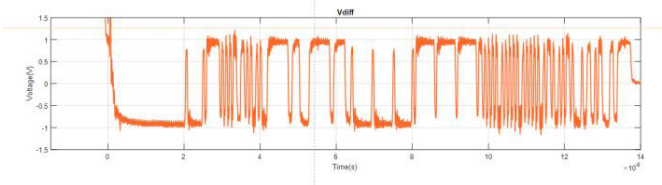


Figure 29: full FAST phase Node 6 transmitting

Result:
Pass at 20Mbit/s

Topology 5c:
CAN like linear topology with 40cm and 1.8m mixed length
Node 8 transmitting, node 3 observation

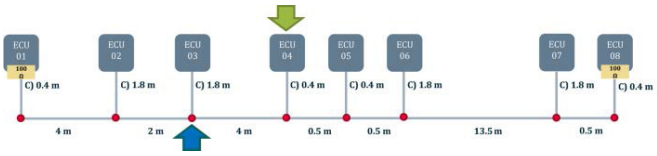


Figure 30: Test Topology 5c

In this topology the stub length of some nodes is extended to 1.8m compared with topology 5a. This longer stub length caused more ringing than in topology 5a which the impact will be shown in the bit rate comparison in the next scenarios.

Scenario 1:
20Mbit/s

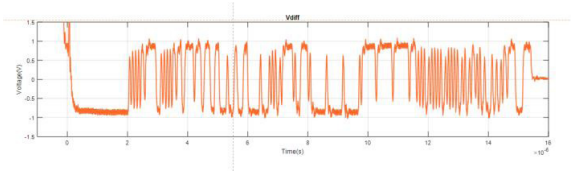


Figure 31: Full FAST phase on node 4 at 20MBit/s

In Figure 31 the FAST mode on node 4 is shown at 20Mbit/s. Voltage level of short bits doesn't achieve the max levels of Level 0 and Level1. The max levels were close to + or -500mV. Due to the difference of the voltage levels of single bits or longer bit phases the bit times are also more asymmetric. In Figure 32 the ADS phase plus the following SDT phase shows the difference of single bit levels and longer bit levels in detail. In case of two consecutive bits the max level could be achieved while a single bit achieves sometimes only 500mV. During the transition level 0 to level 1 or wise versa also reflections as small plateaus can be seen.

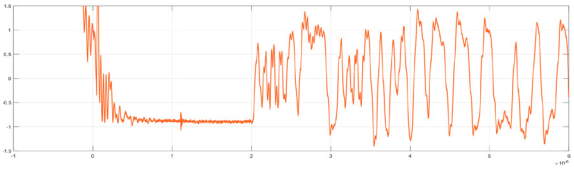


Figure 32: Zoon in AS and SDT field at 20Mbit/s

In Figure 32 a zoom into the ADS and SDT field is shown. In the pattern in the (SDT field), the voltage levels of level 0 and level 1 are in a range of +/- 500mV instead of +/- 1V. Reflections in longer level 0 or level 1 phases were also observed.

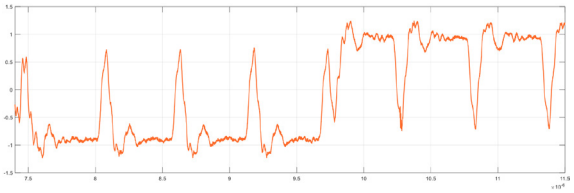


Figure 33: Zoom in pattern field at 20MBit/s

In Figure 33 the worst-case scenario one Bit level after a long stable phase of level 0 or level 1 before is shown. The maximum voltage levels on a single bit are in a range of +/- 500mV instead of +/- 1V. The bit times are shortened and the situation might be critical in case of temperature, wire impedance and Transceiver parameter variation.

Result:
Unacceptable deviation from nominal bit time
Fail at 20Mbit/s

Scenario 2:
Topology 5c at 16Mbit/s

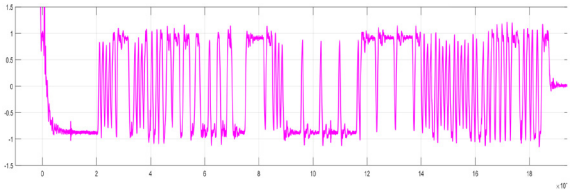


Figure 34: Full FAST Phase on Node 4 at 16MBit/s

In the same network the performance of 16MBit/s was analyzed. In the FAST phase the level of the single bits are higher than at 20Mbit/s but the voltage level doesn't achieve the max levels of Level 0 and Level1. Also, at 16Mbit/s the bit length deviation from the nominal bit time was not acceptable.

Result:
Unacceptable deviation from nominal bit time
Fail at 16Mbit/s

Scenario 3:
Topology 5c 14Mbit/s

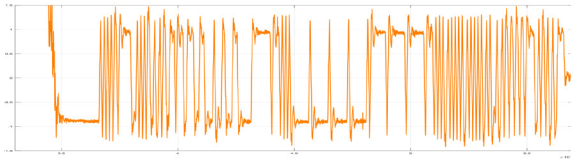


Figure 35: Full FAST Phase on node 4 at 14 MBit/s

At 14 Mbit/s the voltage levels of single bits are in the expected range. doesn't achieve the max levels of Level 0 and Level1. At 14 Mbit/s the bit length deviation from nominal bit time acceptable.

Result:
Pass at 14Mbit/s

Topology 7:

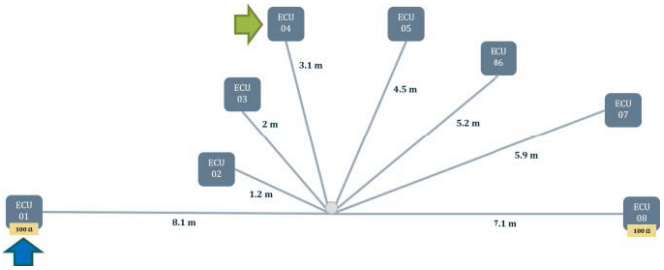


Figure 36: Test Topology 7

Topology 7 is a typical CAN network topology with a star point and long stubs between 1,2m and up to 8,1 m. High bit rates in this topology are not possible. First acceptable results are possible at 8Mbit/s

Scenario:
Topology 7 at 8Mbit/s

Figure 37: Full CAN XL Frame on Node 4

In Figure 37 the complete CAN XL frame is shown including CANH (in blue), CANL (in red), the bus differential signal (in yellow) and the RxD signal (in green.)

Figure 38: SIC to FAST transition ADS SDT Phase

In Figure 38 the SIC to FAST transition is shown. Voltage levels of single bit burst in SDT field are symmetric but strong reflections after level 0 to level 1 transition and vice versa can be seen. The reflections are crossing the 0V line and shortened the bit length. But the Receiver filter out this noise and the timing symmetry of the RXD signal depends on the Receiver filter performance.

Figure 39: Pattern field in FAST phase

In Figure 39 the 1,2,3 bit scenario after 4 consecutive bits is shown. It can be seen, that the time until a reflection is finished is longer than 2-bit times. At the end it could be observed, that

- the asymmetry of the bit time depends on number of bits
- the Plateau during the transitions level 0 to level 1 or vice versa at Vdiff = 0V might cause asymmetry
- The asymmetry on the RXD pin depends on the Receiver Threshold
- Timing symmetry on the RXD pin depends on the Receiver filter performance

Result:
Reflection due to the star point and the long stubs limit the bit rate
8Mbit/s: pass

Topology 8a:
Figure 37: Test Topology 8 scenario 1

Scenario1:

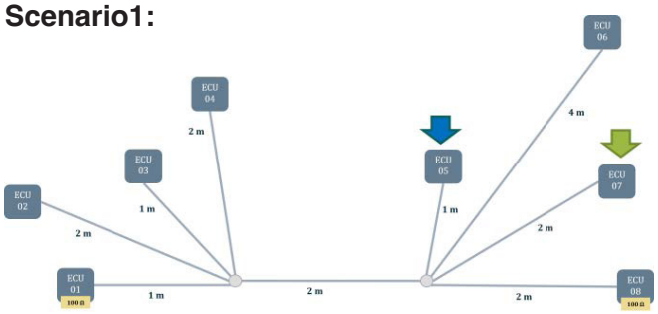


Figure 40: Test Topology 8

Topology 8 is a double star topology which also used in CAN networks. Two stars are available with a distance of 2m and the stub length are 1 m or multi of them (2m and 4m). This is a critical scenario in terms of reflections. The reflected wave can accumulate to high levels on the nodes.

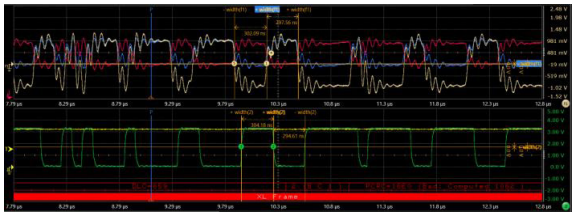


Figure 41: Pattern field at 10MBit/s

Observation:
- Ringing not finished during one bit time
- Impact on timing symmetry expected
- Ringing longer that 2-bit times

Scenario 2:
Node 2 transmitting, node 5 receiving

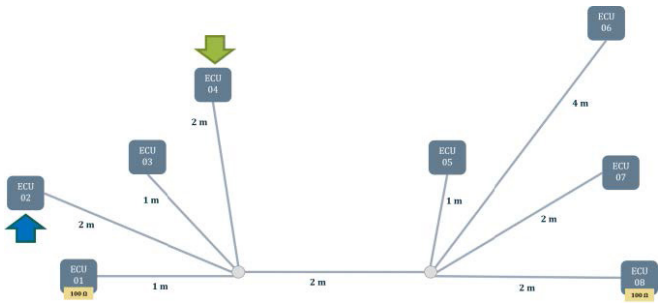


Figure 42: Test topology 8; Scenario 2

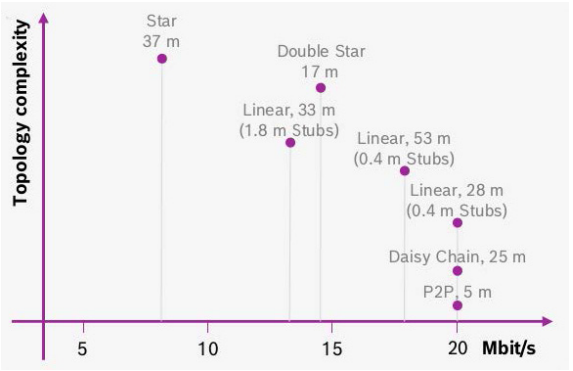
This combination shows less ringing and more robust communication. We had also 13Mbit/s tested but not documented. In all combinations with a bit rate of 13Mbit/s the communication war reliable and robust.

Figure 43: Pattern field at 10MBit/s

Result:
Ringing were observed on the bus but the receiver was able to filter out the noise and on RXD the bit length symmetry was in an acceptable range.

Pass at 13Mbit/s

Results overview of all topology investigations



Conclusion:

With the new transmitter concept of the CAN SIC XL Transceiver and in combination with the CAN XL protocol a high step in terms of bit rates in the data phase are possible. But the max bit rate depends dramatically on the network design and the wire impedance. As more harmonic the impedance in the network is, as higher the possible bit rate can be. Long stub length and a high number of unterminated stubs as well as a high number of star point limits the maximum possible bit rate. Also, the impedance of the wire must be stable in terms of

- Temperature dependency
- Production variation of the impedance
- Pressure dependency of the impedance
- Twist length and number of twists
- Short untwisted parts
- Symmetry of CANH and CANL wire length

The tolerance has an impact on the signal integrity and at the end on the maximum possible bit rate.

Recommendations:
To achieve high bit rates

- ➢ The topology should be as linear as possible
- ➢ As shorter the stubs should be
- ➢ The number of stubs should be less
- ➢ The wire length of CANL and CANH has to be close together
- ➢ The wire impedance has to be 100Ω with a small temperature dependency, production variation and pressure dependency
- ➢ The untwisted part at the end of a wire has to be short
- ➢ The topology should be verified via simulation

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