The physical layer in the CAN XL world
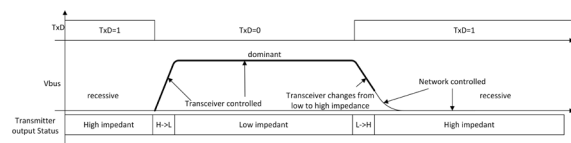
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CAN-XL as an improvement of the well-established CAN FD protocol increases payload and increases the average bit rate in a CAN network up to 12 Mbit/s. This article explains the new CAN XL transceiver approach and concept, the challenges in the networks and how to combine the CAN XL protocol with the existing CAN FD transceiver and CAN SIC Transceiver and the new CAN XL transceiver.

The CAN protocol was first time published more than 35 years ago and 25 years later, the first discussion about an improvement called CAN FD was started. After the successful release of the CAN FD protocol, the corresponding physical layer standard specifications and the availability of CAN FD transceivers and microcontroller supporting CAN FD, it was time to initiate the next level called CAN XL. The main motivation was to increase the payload. Starting from 8 Byte in CAN and up to 64 Byte in CAN FD, CAN XL is doing a big step up to 2k Byte. To reduce the transmitting time for such a big payload, higher bit rates are needed to achieve acceptable times. Transmitting a CAN Frame with 2k Byte data with a bit rate of 500kBit/s needs 33ms. A CAN FD Frame transmitted with 500 kBit/s in the arbitration phase and 2000kBit/s in the data phase and a payload of 2k Byte data needs more than 8ms. For automotive applications, this transmitting times for CAN frames is too long and so the target was to achieve 2ms. To achieve this transmitting time with 2k Byte payload, a bit rate of 10 Mbit/s and higher in the data phase is necessary. 500kbit/s in the arbitration phase are set to allow the same distances between ECUs in networks like with CAN FD.

The Physical Layer concept in CAN

The CAN bus is a fieldbus and allows more than two nodes connected on a bus. In a fieldbus topology with a higher number of nodes, collisions are possible. To manage these collisions, CAN uses the CSMA/CR (Carrier Sense Multiple Access/ Collision Resolution) concept. In the arbitration phase, one or more nodes can transmit a CAN Frame on the bus at the same time and the node with the highest priority wins the arbitration. To support this CSMA/CR concept, transceivers controlling both levels (TxD=0 and TxD=1) on the bus, cannot be used. In case of a collision, the bus level on the bus will be not defined if one transceiver transmits Level 0 and the other transceiver transmits Level 1 at the same time. During this collision, the transceiver might bedamaged. For that reason, a CAN transceiver controls only one level (TxD=0). This is called dominant level. During the recessive level (TxD=1), the transceiver output stages are high ohmic and the termination resistors are responsible for the recessive state on the bus. In Figure 1 this behavior is demonstrated.

Figure 1: Basic Transceiver transmitter concept

This concept allows a transmitting node to overwrite the recessive state on the bus with a dominant level without the risk to damage a transceiver transmitting a recessive level at the same time. With such a concept, collisions on the bus can be supported. The disadvantage is that the transceiver's output stages are changing from high impedance to low impedance and vice versa. This impedance change creates reflection on the bus.

Reflection in a CAN Topology

In the transmission line theory it is important that the wire impedance and the termination impedance at the end of the wire have the same value. If wire impedance and termination impedance matches, no reflection occurs. If the impedances between the wire and the termination are different, reflection is caused by the different impedances. The formula for reflection is as follows:

$$r = \frac{Zt - Zw}{Zt + Zw}$$

- Z_t is the termination impedance and
- Z_w is the wire impedance.

Table 1: Reflection factor for 120Ω wire impedance

Termination impedance	Reflection factor
30Ω	-0.6
40Ω	-0.5
60Ω	-0.33
120Ω	0
100kΩ (Transceiver input imp.)	+0.99

In Table 1 some numbers for the reflection factors are shown. For termination impedances smaller than the wire impedance, the wave will be reflected at the end of the wire and changes the polarity. If the end of a wire is terminated with a transceiver only (100kΩ), the wave will be fully reflected with an unchanged polarity. On star points, the impedance changes, too. On a star point with 3 stripes (1 line for the incoming wave and two lines for the outgoing wave) the reflection factor is –0.33. The two outgoing lines are in parallel with two times 120Ω impedance and the overall impedance for the wave is 60Ω. These reflections are caused with every transition on a wire, independent if the bus levels are changing from dominant to recessive or vice versa. However, there is one difference. In case of a recessive to dominant transition, the reflection will be damped by the low ohmic transceiver output stages.
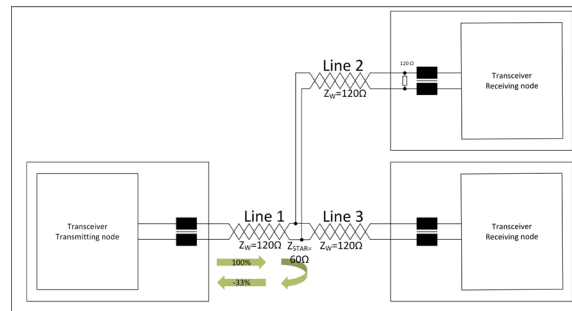

Figure 2: Reflection on a star point

In case of the dominant to recessive transition, the bus is high ohmic and the reflections fade. The length of the fading phase depends on the wire length and the number of stripes. A long fading phase limits the maximum bit rate in the data phase because the sampling point has to be set after the fading is finished in order to get a reliable sampling. To realize higher bit rates, the number of ringing must be reduced and thus the transition from dominant to recessive has to be controlled by the transceiver. This is the concept of the new CAN SIC (Signal improvement capability) transceiver.

CAN SIC (Signal Improvement Capability)

The new CAN SIC transceiver based on the specification CiA 601-4, two solutions are available: transmitter (Tx) based concepts and receiver (Rx) based concepts.

In the Tx based solution, the transmitter controls actively the dominant to recessive transition and afterword's up to 500ns of the following recessive phase. In case of shorter recessive bits, the transmitter changes from active recessive to dominant directly. If the recessive bit is longer, the transmitter changes from active recessive to passive recessive (high ohmic) state like in standard CAN FD transceiver. With CAN SIC transceiver, up to 5 Mbit/s in star topologies and 8Mbit/s in linear topologies are possible.

In the Rx based solution, all nodes suppress the recessive signal after the dominant to recessive transition. The suppression time depends on the product and is optimized for one bit rate. For example for 2 Mbit/s, the transceiver suppression time is up to 450ns long.

Table2: CAN FD and CAN SIC parameter

Parameter	CAN FD TrX ISO11898-2		CAN SIC TrX CiA 601-4	
	Min	Max	Min	Max
Transmitted recessive bit width	① -45ns	⑨ +10ns	① -10ns	⑨ +10ns
Receiver timing symmetry	② -45ns	⑧ +15ns	② -20ns	⑨ +15ns
Received Recessive bit width	-80ns	+20ns	-30ns	+20ns

To achieve higher bit rates, the symmetry parameter of CAN SIC Transceiver are improved. The new parameters are shown in Table 2. The maximum values are the same as in ISO 11898-2:2016, but all minimum values are reduced and allow a higher bit rate. Figure 3 shows the effect for 5 Mbit/s. The tailored parameter for CAN SIC allows a higher range for network effects and the sample point.
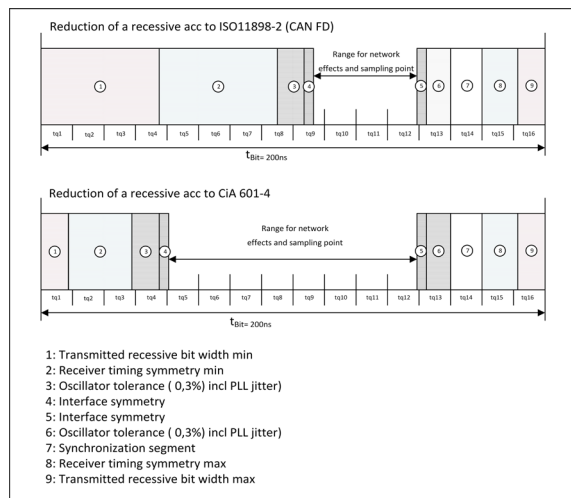

1: Transmitted recessive bit width min
2: Receiver timing symmetry min
3: Oscillator tolerance (0,3%) incl PLL jitter)
4: Interface symmetry
5: Interface symmetry
6: Oscillator tolerance (0,3%) incl PLL jitter)
7: Synchronization segment
8: Receiver timing symmetry max
9: Transmitted recessive bit width max

Figure 3: Bit asymmetry for CAN FD and CAN SIC

The main impact is coming from the min limits for Transmitted recessive bit width, changing from -45ns to -10ns and the receiver symmetry, changing from -45ns to -20ns.

A general disadvantage of the CAN FD and CAN SIC physical layer concept is the asymmetric distance between transmitter levels and receiver thresholds. The distance from the recessive level to the highest possible receiver threshold is 900mV and the distance from the typical dominant level to the lowest receiver threshold is 1.5V. This difference causes conceptual asymmetry for the timings. To achieve high bit rates, another transmitter concept in the data phase is necessary.
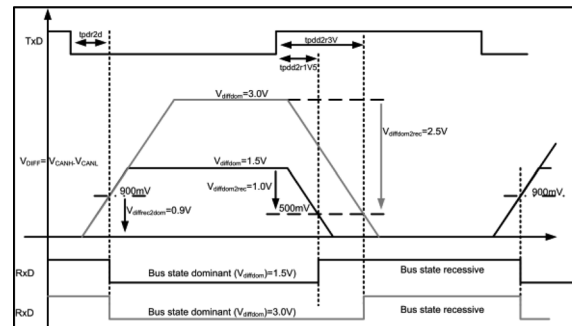

Figure 4: Bit asymmetry caused by dominant level variation

Dual Mode transmitter concept

The main targets for the DM SIC transmitter concepts are:
- Support of CSMA/CR and min 500kBit/s in the arbitration phase
- Same pinning like for CAN FD transceiver
- Support minimum 10 Mbit/s in the data phase
- Reduce the timing asymmetry in data phase

To cover all these requirements for the arbitration phase, the CAN SIC concept is used. In the data phase, an alternating bus voltage concept is used based on the FlexRay idea. The advantage of the FlexRay concept is that the levels are symmetric to the receiver thresholds. The impedances of both levels are close to the wire impedance (less reflection) and the timing asymmetries are very small. The new CAN XL transceiver has now two modes instead of one mode like implemented in all CAN and CAN FD transceiver. The new modes are:
- The Slow Mode (arbitration phase) The slow mode is used in the arbitration phase and based on the CAN SIC transceiver concept. All parameters are accordance with CiA 601-4.
- The Fast Mode (data phase) In the fast mode, the transceiver controls both levels. The bus levels (Vdiff) are alternating between +1V (Level 0) and -1V (Level 1)

The new Fast Mode

In Fast Mode, the transmitter concept changes completely compared to the established CAN and CAN FD transceiver. The output signal will be transmitter as symmetric alternating differential signal. The new levels are named
- Level0 if TxD0
- Level1 if TxD1

The receiver threshold are +/-100mV. The output levels are now symmetric to the receiver threshold and reduces the timing asymmetries of transmitter and receiver.
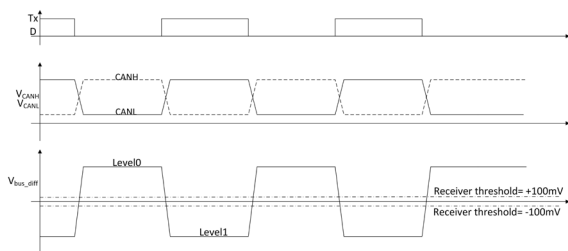

Figure 5: Bus signals in the Fast Mode (Data phase)

The output impedance of the transmitter output stage will be 105Ω for both levels and fits to most used unshielded twisted pair wires. For CAN FD SIC transceiver the output impedances are different for dominant state and active recessive state, and not specified in a standard specification. Transmitter output stage impedances matching with the wire impedances reduce the reflection in a network too. All these parameter are specified in the CiA 610-3 specification. This specification will be released mid of 2020.

The DM SIC transceiver mode changes

The transceiver modes are controlled by the CAN XL controller. Without a mode change, the transceiver can be used as a CAN SIC transceiver only. That allows using the CAN XL transceiver in combination with a CAN FD and/or CAN XL protocol. In the CAN XL protocol two fields are reserved for the transceiver mode switch:
- The ADS field (Arbitration to Data Switch)
- The DAS field (Data to Arbitration Switch)

The ADS field

The ADS field is a part of the control field and located after the arbitration field and before the data field. The ADS field consists of three bits
- AL1 (A=arbitration bit rate), TxD=0
- DH1 (D=data bitrate), TxD=1
- DL1 (D=data bitrate), TxD=0

AL1 is transmitted in arbitration bit rate and during this bit, the transceiver will be switched from slow mode into fast mode.
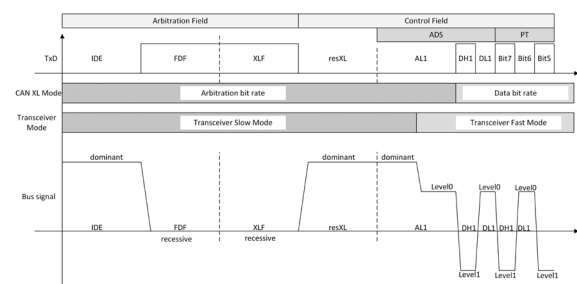

Figure 6: ADS (Arbitration to data) field

The AL1 bit is a dominant bit to guarantee stable signal conditions on the bus with less reflection. After the mode change command from the CAN XL controller, the DM-SIC transceiver switches the receiver thresholds from slow mode threshold levels to fast mode threshold level first. Next, the transmitter of the transmitting node changes the differential bus level from dominant to Level 0. DH1 and DL1 are transmitted with the data bit rate and will be used in the CAN controller for synchronization. In CAN XL, the bit rate switch is not during a bit like BRS bit in CAN FD; the bit rate is switched from AL1 to DH1 bit. The transceiver changes the mode during the AL1 bit.

The DAS field (status Jan 2020)

The DAS field is a part of the Acknowledge field and located between the CRC field and the EOF field. The DAS field consists of three bits
- AH1 (A=arbitration bit rate); TxD=1
- AL2 (A=arbitration bit rate); TxD=0
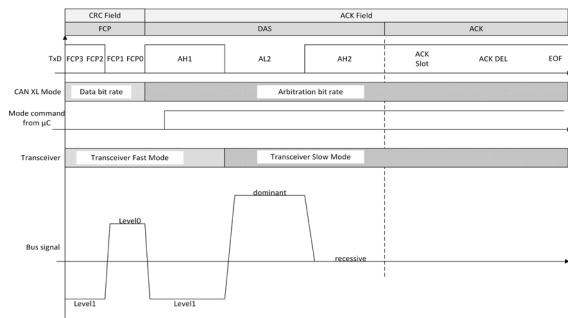- AH2 (A=arbitration bit rate); TxD=1

Figure 7: DAS (Data to Arbitration) field

All bits in the DAS field are transmitted in arbitration bit rate. During the AH1 bit, the transceiver will be switched from fast to slow mode. The AH1 bit will be transmitted with Level 1. After the mode change command, the receiver thresholds will be switch from fast to slow mode first. With the next transition, AH1 to AL2, the transmitter changes from fast to slow mode and the bus voltage levels are changing from Level 1 to dominant level.

Transceiver versus protocol

Most of the users have a strong link in mind between the protocol and the corresponding kind of transceiver (see Figure 8).
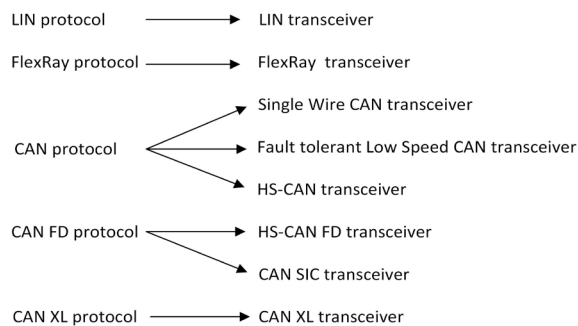

Figure 8: Protocol vs Transceiver

But much more combinations are possible like shown in Figure 9. For the choice of the transceiver concept two topics are important:
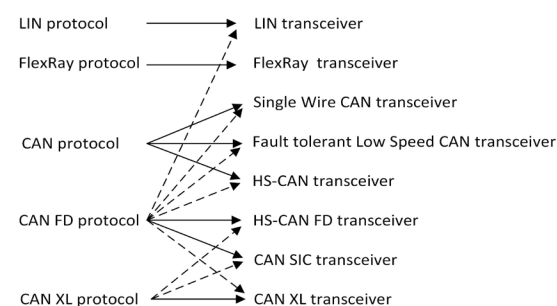- The maximum required bit rate
- The network topology.

Figure 9: Protocol vs Transceiver combination

The protocol has a minor impact on the choice. The exception is, when the Dual Mode of the DM-SIC transceiver should be used. In this case the CAN XL controller is necessary. Only this controller is able to support the dual mode function in the transceiver. The DM-SIC transceiver can also be used in combination with CAN FD and CAN protocol. But in combination the slow mode will be supported only. Below possible combination are listed.

For CAN FD protocol:
- HS-CAN transceiver
- CAN FD transceiver
- CAN SIC transceiver
- CAN XL transceiver (slow mode)

CAN XL protocol:
- HS-CAN transceiver
- CAN FD
- CAN SIC transceiver
- CAN XL transceiver (Dual Mode)
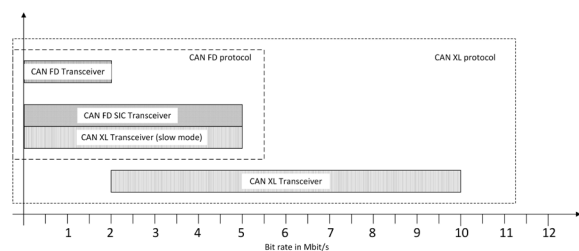
Our proposal for the transceiver choice

Figure 10: Transceiver application area

In Figure 10 recommendation for the bit rate of the different types of transceiver are shown. The max bit rate depends on the network topologies. As higher the number of stubs, stars and nodes, as lower the maximum possible bit rates. Also the ratio between the stubs of a star has an impact of the reflection and the ringing in the network. With the CAN FD and CAN XL protocol and the CAN FD, CAN SIC and DM SIC transceiver, a lot of possibilities are given to achieve the best choice for your application. But the higher bit rates need a very detailed analysis of the network. This can be achieved best by doing network simulations.

Remark:
This article describes the status of the specification discussions in January 2020. Modifications are expected. Updates are available on the CiA homepage.

Annex:

The planned CAN XL specifications:

CiA 610-1:   Datalink layer and physical
              signaling requirements

CiA 610-2:   Datalink layer and physical
              signaling conformance test plan

CiA 610-3:   Physical media attachment sub-
              layer requirements

CiA 610-4:   Physical media attachment
              sub-layer conformance test plan

CiA 610-5:   Media independent CAN
              interface requirements

CiA 610-6:   Media independent CAN
              interface conformance test plan

CiA 610-7:   Higher Layer function
              requirements

CiA 610-8:   Higher Layer function
              conformance test plan

After the release of this specifications they will
be transferred into an ISO specification. Start
planned Q3/2020.

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References
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[2] ISO 11898-2:2016, Road vehicles – Controller
    Area Network part 2: High –Speed-Medium
    access unit, second edition 2016-12-15
[3] CiA 610-1, CAN XL protocol specification (in
    preparation)
[4] CiA 610-3, CAN XL physical layer specification
    (in preparation)